OFFICE OF THE GOVERNOR

January 29, 2024

The Honorable Secretary Gina Raimondo
The United States Department of Commerce
1401 Constitution Ave NW
Washington, DC 20230

RE: California National Semiconductor Technology Center (NSTC) Headquarters

Dear Secretary Raimondo,

I write asking you, the executive leadership of the National Semiconductor Technology Center (NSTC), and Natcast to locate the NSTC Headquarters in California. As the established global epicenter of semiconductor innovation, California's built ecosystem offers the NSTC a world-class launching pad to advance the competitiveness of the U.S semiconductor industry and meet the critical goals of the CHIPS Research and Development Program.

Accessing and Attracting Top Technology Leadership

Building on our Silicon Valley roots, California has the most extensive semiconductor ecosystem comprising industry, entrepreneurs, researchers, workforce training partners, top research universities, national labs, and private investors all coordinating to move ideas from discovery to implementation with speed and efficiency. Unlike anywhere else in the world, California draws a constant stream of leaders with technological acumen who are seeking to leverage and contribute to the engine of innovation here. These dynamics have incubated the most advanced semiconductor technologies and are continuing to push the envelope into next-generation technologies like quantum, artificial intelligence, advanced communications, and new energy solutions.

California has fostered our innovation network and partnered with industry on the nation's most robust R&D tax credit and the establishment of multiple public-private innovation centers that link university researchers with industry partners.

Co-locating the NSTC headquarters within the largest semiconductor brain trust in the world will provide it with consistent access to the critical mass of the state's technology leadership. A California-based HQ has the added advantage of leveraging the constant stream of visiting domestic talent that travels to the state to utilize our research and entrepreneurial assets. A California HQ will brighten the strongest beacon of semiconductor R&D that exists in the world, such that we secure our nation's position as the leader of semiconductor technology into the future.

Asset Management

The NSTC will operate a distributed network of technical centers with capabilities for end-to-end fabrication, pilot runs, small prototyping, and material & equipment testing. For decades, exceptional distributed assets across California have been providing these capabilities to semiconductor innovators across the nation. Examples include Stanford's Nanofabrication Center, UC Berkeley's Marvell Nanofabrication Lab, and the newly announced $4B Applied Materials EPIC Center which provide prototyping and research capabilities via sustainable public-private operational models that have been, and will continue to be, essential resources to researchers. Given the aggressive timeline of establishing an NSTC and the need to protect taxpayer dollars, it will be paramount for the NSTC to utilize the many existing assets housed in California's eight Federally Funded Research Labs and eleven esteemed R1 universities. A California-located NSTC HQ provides NSTC program managers and leadership direct access to the pipeline of researchers from across the nation that rely on our high concentration of facilities. The proximity encourages site visits, enhanced collaboration, and a better iterative process for maintaining the most successful NSTC.

California welcomes the opportunity to work alongside our national network of public and private partners, Natcast, and the NSTC to modernize and expand the impact of our research centers such that we meet the future needs of the industry. Given our shared priority of supporting semiconductor manufacturing and research, this year I signed into law a slate of infrastructure streamlining bills to accelerate construction timelines for our state's most critical projects, including CHIPS-related projects. Working with my Office of Business and Economic Development and our state legislature, we appropriated $120M through our California Competes Grants Program to support awarded CHIPS proposals in the state. The Governor's Office is open and eager to coordinate dialogue with NSTC and industry leadership to identify additional actions that can have an outsized impact on semiconductor innovation and job creation.

Workforce Programming

The semiconductor industry in California employs more than 63,000 people – more than any other state. The enormous workforce presence here is a result of decades-long public and private investments woven into the nation's largest minority-serving higher education systems, undergraduate institutions, and community colleges – institutional knowledge we are eager to share with other regions of the country through HQ operations. We consistently invest in our public education system to deliver the workforce needed to ensure the semiconductor industry's continued growth. The NSTC HQ in California will benefit from direct access to model curricula and hands-on learning experiences created through years of relationship-building between California industry and academic centers.

In alignment with the NSTC, California has prioritized universal and affordable access to career training opportunities for our diverse talent pool. The SEMI Foundation, located in Silicon Valley, is using state grants to develop industry-led training frameworks that will increase high quality job access and equity and can be shared with SEMI members across the nation. Our Labor and Workforce Development Agency has a track-record of working with semiconductor companies, including Applied Materials and Infinera, to develop and fund innovative apprenticeship programs and on-the-job training programs for new and existing hires. By continuing to leverage our academic, industry, and state workforce programs, California can provide the NSTC with replicable partnership and program models to help build the semiconductor technical workforce of tomorrow.

Innovation and Entrepreneurship

Silicon Valley is the recognized global hub where innovators, startups, researchers, and entrepreneurs closely collaborate with private investors to evolve ideas into software and hardware semiconductor solutions for both national defense and commercial applications. California is home to a network of incubators and accelerators, including the world's only semiconductor incubator & accelerator, that are specially equipped to inform the NSTC's mission of facilitating microelectronic innovation. It is our hope that placing the NSTC HQ in our state will broaden access to the experienced VC and private expertise present in California and help deliver the most promising technologies to the marketplace. We strive for a well-equipped NSTC HQ in California capable of bringing together our many localized assets and capabilities, democratizing access to them and expanding the innovation potential of our semiconductor enterprise.

I strongly encourage you to locate the National Semiconductor Technology Center HQ here in California, and my office, alongside a diverse range of stakeholders, is prepared to work in-hand to deliver Natcast and the NSTC with the power to extend America's leadership, optimize pathways from design to production, and develop the semiconductor workforce of the future. As the Department of Commerce and CHIPS Program leadership considers their options, we encourage you to prioritize criteria that mirror the Administration's hallmark values of innovation, diversity, and scientific experience. California is enthusiastic about the opportunities NSTC brings, and we firmly believe that our unique combination of research assets and semiconductor R&D excellence across public institutions and private companies makes California a natural choice to house the NSTC Headquarters.

Sincerely,

Gavin Newsom
Governor of California

C.C. *The Honorable Alex Padilla*
The Honorable Laphonza Butler
The Honorable Nancy Pelosi
The Honorable Zoe Lofgren
The Honorable Doris Matsui
Laurie E. Locascio, National Institute of Standards and Technology (NIST), Director
Eric Lin, CHIPS Research and Development Office, Deputy Director
Jay Lewis, CHIPS Research and Development Office, NSTC Director
Deirdre Hanford, Chief Executive Officer & Trustee, Natcast
Scott Bukofsky, CHIPS Research and Development Office, Director of NSTC Capabilities